Amendments to the Specification:

Please replace paragraph number **0013** with the following amended paragraph:

Some of the system memory may be mapped in the L1 memory address space and some memory may be mapped in the L2 and lower memory address spaces. Every region in memory may be described in a page. A page is a fixed-sized block of memory and the basic unit of virtual memory. The processor 102 may support different page sizes, e.g., 1 kB, 4 kB, 1 MB, and 4 MB. Pages may have properties, e.g., cacheability and protection properties. These properties may be identified by page descriptors such as Cacheability Protection Look-aside Buffer (CPLB) descriptors and Translation Look-aside Buffer (TLB) descriptors. One such descriptor may be a local memory descriptor, e.g., an "L1 ~~LI~~ SRAM" bit, which may be defined on a page-by-page basis and identify a page as being in the L1 logical address space or not, e.g., by being set to "1" or "0", respectively.

Please replace paragraph number **0015** with the following amended paragraph:

If the L1 SRAM bit is "1", indicating that the page is in the L1 address space, the local memory controller 135 sends the access to the L1 SRAM 145 ~~115~~ (block 212). If the address exists in the L1 SRAM 145, the L1 SRAM 145 will return the requested data (block 214).